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CHAE et al.(10) **Pub. No.: US 2017/0098624 A1**(43) **Pub. Date: Apr. 6, 2017**(54) **SEMICONDUCTOR CHIP INCLUDING A PLURALITY OF PADS**(71) Applicant: **SAMSUNG ELECTRONICS CO., LTD.**, Suwon-si (KR)(72) Inventors: **Kwanyeob CHAE**, Hwaseong-si (KR);
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Jin-Ho CHOI, Seoul (KR)(73) Assignee: **SAMSUNG ELECTRONICS CO., LTD.**, Suwon-si (KR)(21) Appl. No.: **15/277,339**(22) Filed: **Sep. 27, 2016**(30) **Foreign Application Priority Data**Oct. 2, 2015 (KR) 10-2015-0139167
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ABSTRACT

A semiconductor chip including a plurality of input/output units includes: a plurality of additional pads disposed on a surface of the semiconductor chip, wherein the plurality of additional pads include at least one of a first additional pad to which a ground voltage is applied and a second additional pad to which a power supply voltage is applied; and a plurality of pads disposed on the surface of the semiconductor chip, wherein the plurality of pads include at least one of a first pad to which the ground voltage is applied and a second pad to which the power supply voltage is applied, and further include a third pad through which a signal is input and/or output. The at least one of the first additional pad and the second additional pad is disposed on an input/output unit where the third pad is disposed, among the plurality of input/output units.

